

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	296	(depth adj reduction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 18:19
L2	5	(depth adj reduction) and (logic adj gate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 18:21
L3	2	("4703435").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 18:21
S1	1313	716/18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:04
S2	1574	716/2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 14:13
S3	1829	716/1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 14:15
S4	772	716/7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 14:15
S5	388	326/104	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:04
S6	276	326/10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:04

S7	0	(716/18).ccls. and ((adder and comparader) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:05
S8	17	(716/18).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:06
S9	7	(716/2).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:06
S10	6	(716/1).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:06
S11	1	(716/7).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:07
S12	0	(326/10).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:08
S13	0	(326/104).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:08
S14	30	("716"/\$).ccls. and ((adder and comparat\$) and depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:09
S15	2	("716"/\$).ccls. and ((adder and comparat\$) and depth) and scalable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:11
S16	168	((adder and comparat\$) and depth) and scalable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:14

S17	1	(adder and comparat\$) and (small adj depth) and scalable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:15
S18	0	(small adj depth) and (scalable adj (logic adj circuit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:16
S19	1	(small adj depth) and (scalable adj (logic adj circuits))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 15:16
S20	0	(logic adj circuit) same ((two adj input) adj gate) same depth	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 16:07
S21	92	(logic adj circuit) same (gate) same depth	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 16:29
S22	0	(logic adj circuit) same (gate) same (reduced adj depth)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 16:29
S23	4	(logic adj circuit) same (gate) same (depth adj reduction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 17:04
S24	9	(logic adj circuit) and (gate) and (depth adj reduction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 17:14
S25	0	(logic adj circuit) and ((two adj input) adj gates) and (depth adj reduction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 17:15
S26	0	((two adj input) adj gates) and (depth adj reduction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/16 18:19

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)
IEEE Xplore®
RESEARCH

 Welcome
 United States Patent and Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

 Your search matched **13** of **1128145** documents.

 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or enter a new one in the text box.

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 Multiconfiguration technique to reduce test duration for sequential circuits
Bertrand, Y.; Bancel, F.; Renovell, M.;

Test Conference, 1993. Proceedings., International , 17-21 Oct. 1993

Pages:989 - 997

[\[Abstract\]](#)
[\[PDF Full-Text \(864 KB\)\]](#)
IEEE CNF
2 Wireless local loop (WLL) based on DCS1800 technology
Westman, T.; Rikkinen, K.; Ojanpera, T.; Tarkiainen, M.;

Local Loop Fixed Radio Access, IEE Colloquium on , 1 Dec 1995

Pages:3/1 - 3/6

[\[Abstract\]](#)
[\[PDF Full-Text \(452 KB\)\]](#)
IEEE CNF
3 FPGA-based digit-serial complex number multiplier-accumulator
Sansaloni, T.; Valls, J.; Parhi, K.K.;

Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 4 , 28-31 May 2000

Pages:585 - 588 vol.4

[\[Abstract\]](#)
[\[PDF Full-Text \(436 KB\)\]](#)
IEEE CNF
4 DCS1800 based wireless local loop (WLL)
Westman, T.; Rikkinen, K.; Ojanpera, T.;

Vehicular Technology Conference, 1996. 'Mobile Technology for the Human Race' IEEE 46th , Volume: 1 , 28 April-1 May 1996

Pages:311 - 315 vol.1

[\[Abstract\]](#)
[\[PDF Full-Text \(396 KB\)\]](#)
IEEE CNF

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE


[Membership](#) | [Publications/Services](#) | [Standards](#) | [Conferences](#) | [Careers/Jobs](#)
IEEE Xplore®
EXPLORING THE FRONTIERS OF KNOWLEDGE

 Welcome
 United States Patent and Trademark Office

[Help](#) | [FAQ](#) | [Terms](#) | [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

[Tables of Contents](#)

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

[Search](#)

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

[Member Services](#)

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

[IEEE Publications](#)

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

 Your search matched **2** of **1128145** documents.

 A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or enter a new one in the text box.

☐ Check to search within this result set

Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **FPGA-based digit-serial complex number multiplier-accumulator**

Sansaloni, T.; Valls, J.; Parhi, K.K.;

 Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 4 , 28-31 May 2000
 Pages:585 - 588 vol.4

[\[Abstract\]](#)
[\[PDF Full-Text \(436 KB\)\]](#)
IEEE CNF

2 **Asynchronous circuit design based on the RTBT monostable-bistable logic transition element (MOBILE)**

Glosekotter, P.; Pacha, C.; Goser, K.F.; Prost, W.; Kim, S.; van Husen, H.; Reimann, T.; Tegude, F.J.;

Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on , 9-14 Sept. 2002

Pages:365 - 370

[\[Abstract\]](#)
[\[PDF Full-Text \(352 KB\)\]](#)
IEEE CNF
[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved


[Web](#) [Images](#) [Groups](#) [News](#) [Froogle](#) [Local](#) ^{New!} [more »](#)

[Advanced Search](#)
[Preferences](#)

Web

 Results 1 - 100 of about 140 for logic gates "depth reduction". (0.53 seconds)

[PDF] A Depth-Decreasing Heuristic for Combinational Logic: How to ...

File Format: PDF/Adobe Acrobat

 ... our basic argument is that heuristic methods can in some cases effect a **depth reduction** from N to ... The **logic** network is made up of two-input Boolean **gates**. ...

portal.acm.org/ft_gateway.cfm?id=123305&type=pdf - [Similar pages](#)

[PDF] LAIS: An Iterative Speedup Heuristic for Mapped Logic

File Format: PDF/Adobe Acrobat

 ... each of the other **gates** in its **logic** class. ... Some **gates** not changed back might be non-critical fsnouts ... log N **depth reduction** starting with AND, OR, XOR and XNOR ...

portal.acm.org/ft_gateway.cfm?id=149572&type=pdf - [Similar pages](#)
[\[More results from portal.acm.org \]](#)

[PDF] 2 (2nn+')

File Format: PDF/Adobe Acrobat

 ... f;(e). Any n-variable r-valued **logic** function f ... consisting of overflow, inhibit, and addition **gates** at a ... lead to a substantial cost and **depth reduction** in the ...

doi.ieeecomputersociety.org/10.1109/12.53584 - [Similar pages](#)

Extending OPMISR beyond 10× Scan Test Efficiency

 ... The 100× scan buffer **depth reduction** shown here applies only to ... for OPMISR in the IBM ASIC Blue **Logic** methodology for ... of up to 72 million wirable **gates** in the ...

doi.ieeecomputersociety.org/10.1109/MDT.2002.1033794 - [Similar pages](#)
[\[More results from doi.ieeecomputersociety.org \]](#)

[PDF] Carry Circuit Depth Optimisation by BDD Based Decomposition

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... decomposition for **depth reduction** based on its BDD implementation ... BDD decomposition mapped into AND-OR basis; gate depth equals 2 ... **Logic** and Architecture Synthesis ...

www.dice.ucl.ac.be/~anmarie/patmos/papers/S4/4_1.pdf - [Similar pages](#)

[PDF] Design for Low Power in Actel Antifuse FPGAs

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... depth to that node, ie the number of **logic gates** from the ... **Logic Depth Reduction** for Frequently Switching Signals By reordering "if - then...else" constructs ...

www.actel.com/documents/lowpower.pdf - [Similar pages](#)

[PDF] Timing-driven logic bi-decomposition - Computer-Aided Design of ...

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... The relevance of field programmable gate arrays (FPGAs ... Bi-decomposition and **depth reduction** are interleaved ... V presents the main algorithm for **logic** decomposition ...

www.lsi.upc.es/~jordicf/gavina/BIB/files/tcad03_bidec.pdf - [Similar pages](#)

[PDF] TIMING OPTIMIZATION

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... Page 29. LATTIS • LATTIS: **Logic** Area-Time Trade-off Integrated circuitS do { ... for each gate on critical path leading to worst_output ... **depth reduction**) ...

athena.ee.nctu.edu.tw/courses/CAD/5_A_Timingoptimization.pdf - [Similar pages](#)